REMARKS

Claim 46 has been amended and claim 7 was previously canceled without prejudice. Applicant respectfully requests reconsideration and allowance of the subject application in view of the amendments and the remarks to follow. Claims 1-6 and 8-53 are pending in this application.

The amendment to claim 46 renders the usage of the term "nonvolatile" consistent with such usage in other claims. The amendment to the specification adds a dictionary definition of the term "exposes" consonant with the usage of the term in Applicant's claims, in response to confusion noted on the record. No new matter is added by the amendments to the claims or the specification.

Amendment to provide clear definition of terminology is permitted, as discussed in MPEP §2163.07, entitled "Amendments to Application Which Are Supported in the Original Description". This MPEP section states that "Amendments to an application which are supported in the original description are NOT new matter." In a subsection I, entitled "REPHRASING", this MPEP section states that:

> Mere rephrasing of a passage does not constitute new matter. Accordingly, a rewording of a passage where the same meaning remains intact is permissible. *In re Anderson*, 471 F.2d 1237, 176 USPQ 331 (CCPA 1973). The mere inclusion of dictionary or art recognized definitions known at the time of filing an application would not be considered new matter. If there are multiple definitions for a term and a definition is added to the application, it must be clear from the application as filed that applicant intended a particular definition, in order to avoid an issue of new matter and/or lack of written description. See, e.g., *Schering Corp. v. Amgen, Inc.*, 222 F.3d 1347, 1352-53, 55 USPQ2d 1650, 1654 (Fed. Cir. 2000).

Accordingly, the amendment to the specification does not comprise new matter.

The Examiner's approval of the amendments to Fig. 3, as tendered with the Response filed on December 23, 2003, is respectfully requested. Revised formal drawing was enclosed with that Response under separate cover addressed to the Chief Draftsperson. Clarification of the status of the drawing is respectfully requested (e.g., using the "check box" appearing on the Office Action Summary sheet at item 10).

35 U.S.C. § 112

The Office Action states (p. 3, item 3) that "Where applicant acts as his or her own lexicographer ...." The Office Action states that the term "exposes" in claims 2, 20, 30 and 41 is used to mean "contains", and that the accepted meaning is "shows" and then states that Applicant's usage gives rise to indefiniteness in those claims. Applicant finds this puzzling at least in part because the Office Action does not state that such claims are rejected on indefiniteness grounds. Clarification is **again** requested.

Further, the interpretation of the usage of the term "exposes" postulated in the Office Action (p. 3) is incomprehensible to Applicant. These claims respectively recite:

"the file system **exposes** a set of application program interfaces **that are used by an application**" (claim 2);

"An operating system for an integrated circuit (IC) module, comprising: a file system to manage access to data files stored in both volatile memory and nonvolatile memory; and an **application program interface** (API) to **expose** the **file system to applications**" (claim 20);

"**exposing functions to manipulate the data files**, the same functions being used regardless of whether the data files are located on the volatile memory or the nonvolatile memory" (claim 30); and

"**exposing a common set of functions to manipulate** both the volatile data files and the nonvolatile data **files**" (claim 41).

The Office Action states (p. 26, 27) that the Examiner is unable to find any instances of the use of the word "expose" in the specification. Applicant has

previously stated on the record that such is described in the specification at least at p. 5, line 18 et seq.

Examples of the use of the term "expose" taken from Applicant's specification include p. 2, line 16 et seq., which is reproduced hereinbelow in order to assist the Examiner:

> An integrated circuit (IC) module allows volatile data generated by applications to be stored within volatile data files in the volatile memory. A file system tracks the location of all data files as residing in either volatile memory or nonvolatile memory. The file system then facilitates access to the volatile data files in volatile memory in a manner similar to accessing nonvolatile data files in nonvolatile memory.
>
> The file system **exposes** a set of application program interfaces (APIs) **to allow applications to access the data files.** The same APIs are used to access both volatile data files and nonvolatile data files. When an application requests access to a data file, the file system initially determines whether the application is authorized to gain access to the data file. If it is, the file system next determines whether the data file resides in volatile memory or nonvolatile memory. Once the memory region is identified, the file system identifies the physical location of the data file within that memory region.

Additional discussion of the term "expose" is found, as previously noted, at page 5, line 18 et seq., and is reproduced hereinbelow, again in order to assist the Examiner:

> One or more applications 112 and an operating system 114 are stored in ROM 108. Some applications as well as parts of the operating system can reside in EEPROM as well. When the smart card is coupled to a card reader and receives power, the application(s) 112 and operating system 114 are executed on the processor 102. The operating system 114 **exposes** a set of application program interfaces (APIs) that enable resident applications 112 to perform tasks and manipulate data on the smart card. In addition, one or more nonresident applications 116, which execute external to the smart card (e.g., programs on kiosks, point-of-purchase machines, etc.), may also place function calls with the operating system 114 to perform tasks or manipulate data on the smart card. Examples of such tasks include access security,

> cryptographic functions (e.g., encryption, decryption, signing, and verification), file management, commerce, and so forth. One suitable operating system is the "Windows for Smart Card" operating system from Microsoft Corporation.

Applicant is unable to envision how the definition or interpretation contained in the Office Action could possibly comport with the subject matter recited in these claims. Clarification is requested.

Put another way, the interpretation provided in the Office Action appears to give the term "exposes" a meaning repugnant to the ordinary meaning of the term. Such is improper, as is explained below in more detail with reference to MPEP §2111.01, entitled "Plain Meaning". This MPEP section states that "THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS THEY ARE DEFINED IN THE SPECIFICATION". Such is also explained in more detail as noted below:

> While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989) (discussed below). One must bear in mind that, especially in nonchemical cases, the words in a claim are generally not limited in their meaning by what is shown or disclosed in the specification. It is only when the specification provides definitions for terms appearing in the claims that the specification can be used in interpreting claim language. *In re Vogel*, 422 F.2d 438, 441, 164 USPQ 619, 622 (CCPA 1970).

The Examiner indicates (page 27) that "The Examiner requests further guidance on which of these definitions is used for the word "expose" in these claims and strongly recommends that the Applicants find other phrasing for these claims to more clearly set forth their meaning." Applicant notes that the usage of

the term in these claims is consistent with that used in many other U.S. Patents and Patent Applications, and also notes that 35 U.S.C. §112, 2ND ¶ clearly states that: "The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter **which the applicant regards as his invention**." Accordingly, Applicant is entitled to employ claim language in a fashion consistent with dictionary definitions and terms of art. Applicant notes an abundance of published applications and patents employing such language. Applicant further notes that such is available to the Examiner via the search capabilities of the USPTO web site.

Furthermore, why would the Examiner provide such a strained interpretation of the term as used in Applicant's claims, yet appear to comprehend usage of the term as employed, for example, in Ginter et al., U.S. Patent No. 6,427,140, as relied upon by the Examiner in rejecting Applicant's claims? Ginter uses the term "expose" or other similar words employing a common root in numerous locations and contexts, to have different meanings.

For example, Ginter uses the term "exposure" to mean "experience" (e.g., col. 19, line 67 et seq., stating "Acceptance of terms and conditions related to certain electronic content may be direct and express, or it may be implicit as a result of use of content (depending, for example, on legal requirements, previous **exposure** to such terms and conditions, and requirements of in place control information).". Ginter also uses the term "expose" to mean "publicly available" (e.g., col. 21, line 63 et seq., stating "VDE may employ tagging related security techniques, the time-ageing of encryption keys, the compartmentalization of both stored control information (including differentially tagging such stored

information to ensure against substitution and tampering) and distributed content (to, for many content applications, employ one or more content encryption keys that are unique to the specific VDE installation and/or user), private key techniques such as triple DES to encrypt content, public key techniques such as RSA to protect communications and to provide the benefits of digital signature and authentication to securely bind together the nodes of a VDE arrangement, secure processing of important transaction management executable code, and a combining of a small amount of highly secure, hardware protected storage space with a much larger "exposed" mass media storage space storing secured (normally encrypted and tagged) control and audit information."; see also col. 23, line 38 et seq.).

Ginter further uses the term "expose" to mean "to show" or "to make available" (e.g., col. 33, line 36 et seq., stating "A feature of the present invention enables such flexibility of metering control mechanisms to accommodate a simultaneous, broad array of: (a) different parameters related to electronic information content use; (b) different increment units (bytes, documents, properties, paragraphs, images, etc.) and/or other organizations of such electronic content; and/or (c) different categories of user and/or VDE installation types, such as client organizations, departments, projects, networks, and/or individual users, etc. This feature of the present invention can be employed for content security, usage analysis (for example, market surveying), and/or compensation based upon the use and/or **exposure** to VDE managed content.").

Ginter as well uses "expose" to mean "to show or make accessible" (see, e.g., col. 63, line 65 et seq., stating that "It is also possible to analyze and "reverse

engineer" the "die" itself (e.g., using various types of logic analyzers and microprobes to collect and analyze signals on the die while the circuitry is operating, using acid etching or other techniques to remove semiconductor layers to **expose** other layers, viewing and photographing the die using an electron microscope, etc.)").

Ginter further uses the term "exposed" to mean "subjected to" or "to make available to" (e.g., col. 64, line 8 et seq., stating that "For example, ion implantation and/or other fabrication techniques may be used to make it very difficult to visually discern SPU die conductive pathways, and SPU internal circuitry may be fabricated in such a way that it "self-destructs" when **exposed** to air and/or light.").

Additionally, Ginter uses the term "exposure" to mean "availability" (e.g., col. 73, line 21, stating "information control structures protected from **exposure**" as a portion of security description).

Further, Ginter uses the term "exposure by" to mean "access to" (e.g., col. 77, line 28 et seq., stating that "ROS 602 provides mechanisms to protect information control structures from **exposure** by end users and conduit hosts."). Ginter also uses "exposure of" to mean "access to" (see, e.g., col. 87, line 60 et seq., stating that "Validation/correlation tags are typically passed only in secure wrappers to prevent plaintext **exposure** of this information outside of SPU 500."

Moreover, Ginter uses the term "exposure" to mean "visibility" (e.g., col. 132, line 28, stating "Putting keys in distributed objects 300 increases the **exposure** to attempts to defeat security mechanisms by breaking or

cryptoanalyzing the encryption: algorithm with which the private header is protected (e.g., by determining the key for the header's encryption).").

Ginter further uses "exposed" to mean "viewable" (e.g., col. 194, line 36 et seq., stating that "Extraction of content differs from release in that the content is never **exposed** outside a secure container.").

Accordingly, the term "expose", as it is ordinarily used in the English language, is capable of more than one meaning, definition or connotation, even within a single document. Applicant's use of the term "expose" is consistent with the ordinary meanings of the term. The interpretation provided in the Office Action is not consistent with the ordinary meanings of the term, as evidenced by the references being applied by the Examiner, by Applicant's specification, the confusion noted in the Office Action and by dictionary definitions of the term.

Thus, for at least these reasons, Applicant respectfully submits that claims 32, 38, 42 and 45, as presented and as amended, comply with 35 U.S.C. §112, and that claims 2, 20, 30 and 41 also comply with such statute. As such, any rejections or objections on indefiniteness grounds should be withdrawn. Applicant respectfully notes that claims 2, 20, 30, 32, 38, 41, 42 and 45 comply with 35 U.S.C. §112, and that claims 2, 20, 30, 32, 38, 41, 42 and 45 should be allowed.

35 U.S.C. § 102

Claim 1 stands rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,421,279 B1 to Tobita et al. (hereinafter "Tobita"). The Office Action also presents argument (p. 3, item 5) indicative that the Examiner contemplates rejection of claim 8 as being anticipated. Clarification of the rejection and correction of the record are respectfully requested. Applicant respectfully disagrees with the rejection and requests reconsideration.

Anticipation is a legal term of art. Applicant notes that in order to provide a valid finding of anticipation, several conditions must be met: (i) the reference must include every element of the claim within the four corners of the reference (see MPEP §2121); (ii) the elements must be set forth as they are recited in the claim (see MPEP §2131); (iii) the teachings of the reference cannot be modified (see MPEP §706.02, stating that "No question of obviousness is present" in conjunction with anticipation); and (iv) the reference must enable the invention as recited in the claim (see MPEP §2121.01). Additionally, (v) these conditions must be simultaneously satisfied.

Tobita is directed (see, e.g., Title) to a "flash memory control method and apparatus processing system therewith". Tobita teaches (see Abstract) that "A semiconductor file system features a first nonvolatile memory electrically erasable, a second nonvolatile memory not electrically erasable, a volatile memory, a controller, and a control section which controls the controller wherein a physical address corresponding to a logical address specified from an external system is accessed. The first nonvolatile memory stores data for the external system to perform operations, first management information indicating

correspondence between physical and logical addresses, and second management information indicating a state of the first nonvolatile memory. The second nonvolatile memory previously stores interface information. The controller determines a physical sector address. The control section is for controlling input/output of data from/to the external system and for temporarily storing write data into the first nonvolatile memory from the external system in the volatile memory and then transferring the write data from the volatile memory to the first nonvolatile memory."

In contrast, claim 1 recites "An integrated circuit (IC) module comprising: a processor; volatile memory and nonvolatile memory operatively coupled to the processor; and a file system to manage access to one or more data files stored in the volatile memory and in the nonvolatile memory", which is not taught or disclosed by Tobita.

Applicant's specification states (page 5, line 3 et seq.) that:

> Generally, an IC module includes some form of processing capabilities, as well as limited volatile and nonvolatile memory. IC modules typically do not have their own power supply, but instead rely on an external power source, such as power provided by a card reader. In this manner, processing tasks are accomplished only when power is applied to the IC module. In other implementations, the IC modules may be implemented as USB Keys, built-into a motherboard of a computer or even inside of a larger microprocessor or ASIC (Application Specific Integrated Circuit). For discussion purposes, the IC module is described in the context of a smart card.

Tobita is silent with respect to any IC module. In fact, Tobita is void of the term "module".

The Office Action cites (pp. 3, 4) diverse portions of Tobita as providing the various elements described with reference to claim 1. Applicant notes that Tobita describes a number of different embodiments (see, e.g., Brief Description,

col. 14, line 5 though col. 18, line 12, referring to one hundred and three separate Figures). More specifically, Figs. 1-48 are explicitly stated to relate to a first embodiment, Figs. 50-60 are explicitly stated to relate to a second embodiment, Figs. 61-81 are explicitly stated to relate to a third embodiment and Figs. 49 and 82-103 are explicitly stated to relate to a fourth ("forth" as described in Tobita) embodiment. Within this context, Tobita provides numerous different alternative examples or sub-embodiments.

To clarify the legal meaning of the term "anticipation", Applicant notes the language of 35 U.S.C. §103(a):

> A patent may not be obtained though the invention is not **identically disclosed or described** as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This language sets forth Congressional intent in clear and exact terms as to what does or does not comprise anticipation, as compared to unpatentability. The reference must contain, within its four corners, **exactly** the subject matter of the claim, as it appears in the claim, in order to support a valid finding of anticipation.

It is thus inappropriate to combine elements "picked and chosen" from diverse embodiments in attempting to arrive at a finding of anticipation. In part, this is because a finding of anticipation involves determining that the subject matter recited in the claim is already in the public domain, using the rules of evidence set forth in the statute and which are further interpreted in the MPEP and case law. In order to provide evidence of anticipation, the reference must, within

its four corners, set forth this subject matter (item (ii) supra) and enable (item (iv) supra) exactly as it appears in the claim.

In other words, selecting elements from diverse portions of the reference comprises impermissible modification of (e.g., addition to) the teachings of the reference (i.e., see item (iii) supra). Further, because none of items (ii)-(iv) needed in order to provide a valid finding of anticipation are met, item (v) cannot be met. The rejection of claim 1 fails at least four necessary criteria needed in order to determine that the subject matter of the claim is anticipated. This is explained in the last Response (dated Dec. 23, 2003) in more detail.

The Office Action states (p. 27, item 65) that "Claim 1 is extremely broad and appears to be no more than a description of a computer. Many different computers would fit this description." and proceeds to identify various words within Tobita, while ignoring the legal arguments that Applicant has provided regarding the nature of anticipation.

Applicant has provided no fewer than five different legal arguments regarding anticipation and the rejection of claim 1 in the Response dated December 23, 2003. The Office Action responds to none of these legal arguments.

Applicant further notes that it is well established that old elements may be combined to provide results not suggested by references and thereby to be patentable. "The patentability of such combinations is of ancient authority." *Prouty v. Draper*, 41 U.S. (16 Pet.) 336, 341 (1842); *Eames v. Godfrey*, 68 U.S. (1 Wall.) 78,79-80 (1863); *Gill v. Wells*, 89 U.S. (22 Wall.) 1, 25 (1874); see also H.T. Markey, Why not the Statute?, 65 J. Pat. Off. Soc'y., 331, 333-34 (1983) ("virtually all inventions are 'combinations', and ... every invention is formed of

'old elements' .... Only God works from nothing. Man must work with old elements"). These principles of patent law are repeated in many other cases, including *In re Wright*, 6 USPQ2d 1959 (CAFC) and *Fromson v. Advance Offset Plate, Inc.*, 225 USPQ2d 26 (CAFC).

The latter case further states that "There is no basis in the law, however, for treating combinations of old elements differently in determining patentability. See *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d at 1540, 218 USPQ at 880." As noted in *Diamond v. Chakrabarty*, 206 USPQ 193, 196, the Supreme Court stated that "We have also cautioned that courts "should not read into the patent laws limitations and conditions with the legislature has not expressed." *United States v. Dubilier Condenser Corp.*, 289 U.S. 178, 199, 17 USPQ 154, 162 (1933)."

As a result, demonstrating that some of the elements recited in a claim are found in the prior art does not provide a basis for a rejection, and does not provide a basis for anticipation. Accordingly, the anticipation rejection of claim 1 is prima facie defective and should be withdrawn and claim 1 should be allowed.

Claim 8 recites "An integrated circuit (IC) module as recited in claim 1, further comprising at least one application stored in the nonvolatile memory and executable on the processor to request access to the one or more data files", which is not taught or disclosed by Tobita.

The Office Action cites col. 6, lines 52-55 as teaching this aspect of the claimed subject matter. Col. 6, lines 52-55 states that: "If all the above-mentioned points are implemented, the three types of memory can cover various applications and the number of parts can be reduced compared with installation of a memory for each application." "Application", as employed in this passage, does not refer

to any "application ... executable by the processor" or to such that is executable "to request access to the one or more data files" as recited in claim 8. It is a reference to a field of deployment for the overall system, for example, information processing (col. 1, lines 20-22; in conjunction with miniaturized IC cards, col. 6, line 56). Applicant notes that the Examiner fails to respond to this rebuttal of the earlier rejection.

Tobita uses the word "application" exactly thirteen times. The first use of the word "application" relates to foreign priority, while the second through seventh instantiations refer to provenance data.

The eighth and ninth instantiations (col. 6, lines 53 and 54) clearly deal with a range of applications for the information processing system, i.e., field of deployment, and include the instance that is mischaracterized in the Office Actions. The tenth (col. 49, line 52) makes reference to a flash memory application or field of deployment, i.e., consistent with how Applicant has characterized the usage of the term as referring to scope of field of deployment. The eleventh (col. 34, lines 14-16) appears to describe application of the disclosure associated with Fig. 53 to another use. The twelfth instance (col. 48, lines 42 and 43) clearly refers to application of a well-known set associative method to a problem to be solved. The thirteenth example (col. 49, lines 51 and 52) refers to application of a memory to a task.

Not one of these instantiations employs the word "application" in the manner in which the Examiner is choosing to interpret the usage of the word, yet Tobita contains 60 columns of specification directed to application, i.e., usage, of flash memories. Tobita is not concerned with user application programs and

instead is focusing more at a machine language level description of computer operations. No instance of any reference to anything that would or even could be a user application program is identified anywhere in this or the prior Office Action.

Tobita consistently refers to execution of tasks by a CPU and frequently employs the term "flow" with reference to a sequence of computer-executed tasks (see, e.g., col. 15, lines 45 and 46, stating that "FIG. 42 is a sequence flow of garbage collection according to first embodiment of the present invention"; Tobita makes numerous other references to flow etc.).

Tobita is a lengthy document taking priority from a number of Japanese applications and lists a number of inventors who are resident in Japan. As a result, one might realize that the party or parties who prepared the English language specification were not native English speakers and may well not even be familiar with the interpretation of the term "application" as it is being interpreted in the Office Action. Put another way, there is no credible evidence in support of the strained interpretation offered in the Office Action and there is substantial credible evidence for Applicant's interpretation of the usage of the term.

The Office Action also cites col. 45, line 66 through col. 46, line 8 as providing teaching of this affirmatively-recited aspect of the subject matter of claim 8. This passage, which previously reproduced with reference to claim 1, is void of any mention of the word "application" and as such cannot possibly provide the subject matter for which it is cited. The Examiner fails to respond to this argument as well.

The Office Action cites (p. 3) col. 19, lines 65 through col. 20, line 3 as providing "... and executable on the processor ...", as recited in claim 8, where the first ellipsis corresponds to "at least one application stored in the nonvolatile memory ..." and the second ellipsis corresponds to "to request access to the one or more data files", also as recited in claim 8.

Col. 19, line 65 through col. 20, line 3 refers to the first embodiment (col. 18, line 19) and thus this passage is disjoint from the other portions cited in conjunction with rejection of claim 8 and accordingly is inapposite thereto with respect to anticipation. Again, the Examiner fails to respond to this legal argument.

Further, the paragraph extending from col. 19, line 63 to col. 20, line 10 (copy provided in the Response dated Dec. 23, 2003), which includes this passage, provides no teaching or disclosure of the subject matter which it is cited as representing. Clarification is **again** requested.

The anticipation rejection of claim 8 thus also fails all five prongs of the tests noted above. As a result, the anticipation rejection of claim 8 is clearly prima facie defective and should be withdrawn, and claim 8 should be allowed.

35 U.S.C. § 103

Claims 2, 20 and 21 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of U.S. Patent No. 6,519,594 B1 to Li (hereinafter "Li"). Claims 3, 22-27 and 39-42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Li and further in view of U.S. Patent No. 6,542,955 B1 to Chen (hereinafter "Chen"). Claims 4-6, 10-14, 18, 29 and 32 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Chen. Claims 15, 16, 19, 30 and 31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Chen and further in view of Li. Claim 9 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of U.S. Patent No. 6,587,873 B1 to Nobakht et al. (hereinafter "Nobakht"). Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Chen and further in view of Nobakht. Claims 28, 33, 34, 37, 38, 43 and 45 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Li and further in view of Nobakht. Claims 35, 36 and 44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Li and Nobakht and further in view of Chen. Claims 46, 47, 52 and 53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Ginter et al., U.S. Patent No. 6,427,140, hereinafter "Ginter"). Claims 48-51 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Tobita in view of Ginter and further in view of Chen. Applicant traverses and requests reconsideration.

In responding to such a rejection, it is helpful to first review the subject matter addressed by the references. Tobita has been at least partially discussed above with reference to the response to the anticipation rejection.

Li describes "computer-implemented sharing of java classes for increased memory efficiency and communication method" (Title). More specifically, Li states (Abstract) that:

> A computer-implemented method and system for allowing Java classes to be shared among many Java virtual machines (JVMs) including a communication system allowing Java and native applications to readily interoperate. An implementation of the JVM on an operating system platform, e.g., the Aperios AV/OS, allows a variety of applications including desktop applications, applets and Internet based applications, home networking applications, MHEG-6 applets, gaming, gaming applications and next generation audio visual applications to operate with the operating system. The present invention provides a shared memory pool (SMP) into which a JVM and store and register a particular Java class. The stored and registered Java class is then accessible by other JVMs using the SMP and a Java layer class manager that is implemented in software. The Java layer class manager requires other JVMs to access a key for the stored class in order to synchronize access to the Java class among several installed and operating JVMs of the computer system. By sharing common Java classes in this fashion, the memory resource overhead required to operate multiple JVMs on a common computer system is drastically reduced thereby allowing a multiple JVM platform to be operable on an embedded computer system. A novel communication method is also disclosed for communicating information between a JVM application and a native application using the computer system's operating system. The novel communication method also allows multiple JVM applications to communicate using the shared memory pool. These functions are incorporated into a JavaLayer that supports the full PersonalJava™ platform.

In contrast, claim 2 recites "An integrated circuit (IC) module as recited in claim 1, wherein the file system exposes a set of application program interfaces that are used by an application to request the one or more data files stored in the volatile memory and the nonvolatile memory", independent claim 20 recites "An

operating system for an integrated circuit (IC) module, comprising: a file system to manage access to data files stored in both volatile memory and nonvolatile memory; and an application program interface (API) to expose the file system to applications" and claim 21 recites "An operating system as recited in claim 20 wherein the API defines a function for opening a data file, the function being used to open data files in the volatile memory and the nonvolatile memory".

The portions (col. 4, lines 58-60 and col. 31, lines 32-54) of Tobita cited in the Office Action (p. 13, item 28) as providing "... a file system to manage access to data files ...." are explicitly stated to use a flash memory, i.e., a nonvolatile memory, as a storage medium. Col. 4, lines 58-60 states that: "It is therefore an object of the invention to provide a file system using a high-performance and inexpensive flash memory as storage media." In contrast to both the Office Action and Tobita, claim 20 recites "a file system to manage access to data files stored in **both** volatile memory and nonvolatile memory". As noted above, Tobita teaches use of volatile memory as a write buffer and thus has no need to manage access to data files stored in both volatile memory and nonvolatile memory. The latter passage describes temporary use of SRAM as a write buffer 2006 to aid in the speed with which files can be transferred from a host to flash memory and does not describe a file system as recited in claim 20.

The portion (col. 45, line 66 through col. 46, line 8) of Tobita cited (p. 15) in the Office Action as providing a portion of the affirmatively-recited "file system to manage access to data files stored in both volatile memory and nonvolatile memory ..." of claim 20 refers (see col. 45, line 64 et seq.) to a fourth embodiment again involving use of RAM for temporarily storing (see col. 46, line 6) data as a

step towards storage of the data in nonvolatile memory for subsequent access. This passage merely describes a cache memory for a write buffering system in conjunction with a fourth embodiment of the disclosure of Tobita. There is no suggestion or motivation identified by the Office Action within Tobita to "mix and match" diverse aspects of the disclosure of Tobita. As noted elsewhere, 'obvious to try' is not an appropriate standard for a finding of unpatentability, and hindsight reconstruction is similarly inapposite to a legal determination of unpatentability.

More specifically, the passage beginning at line 63, col. 45 states that:

> Embodiment 4
>
> A fourth embodiment of the invention is described with reference to the accompanying drawings.
>
> FIG. 82 is a block diagram of an information processing system according to the fourth embodiment of the invention, wherein numeral 4001 is a CPU (central processing unit) which executes programs and processes data, numeral 4002 is a flash memory which is a large-capacity **nonvolatile memory storing the programs, data**, etc., handled by the CPU 4001, and numeral 4003 is a **cache memory which is a volatile memory temporarily storing data such as data transferred from the flash memory and write data from the CPU** 4001. The cache memory 4003 can be made of a DRAM (dynamic random access memory), an SRAM (static random access memory), or the like, for example. Numeral 4004 is an address array for recording CPU addresses assigned to data stored in the cache memory 4003, which are output by the CPU to access the data, and their appendant [sic] information. Numeral 4005 is an address comparison circuit for comparing the address corresponding to the data whose access is requested by the CPU 4001 with the addresses recorded in the address array 4004. Numeral 4006 is a controller which controls the information processing system so that accurate data can be accessed at high speed as much as possible in response to an access request made by the CPU 4001. Numeral 4007 is a memory bus of the CPU 4001. The address array 4004, the address comparison circuit 4005, and the controller 4006 can be made of electronic devices such as CMOS (complementary metal oxide semiconductor) transistors, resistors, ROM which stores predetermined processing programs, RAM, and CPU. In the description that follows, assume that the address space in which addresses accessed by the CPU 4001 exist is allocated to the flash

> memory 4002. Numeral 4060 is input means having at least a function for an external system including the user to enter commands such as data access commands and addresses; for example, it is implemented by a mouse or keyboard. Numeral 4061 is means having an output function of messages (described below) and necessary information; it can be implemented by print means such as a printer or display means such as a CRT, EL display, or liquid crystal display.

This passage does not provide, suggest or motivate any "file system to manage access to data files stored in both volatile memory and nonvolatile memory" as recited in claim 20.

The portions (col. 4, lines 58-60 and col. 6, lines 52-55) of Tobita cited (p. 15) in the Office Action as corresponding to "... to expose the file system to applications ..." respectively refer to flash memory and multiple memories but are void of any mention of anything recognizably related to "an application program interface (API) to expose the file system to applications", as recited in claim 20. This passage has no discernible relationship to the subject matter of claim 20. Clarification of the rejection is respectfully requested.

The Office Action also cites col. 5, lines 52-55 with respect to this portion of claim 20. Col. 5, lines 50 et seq. states that: "the first management information, and the second management information for controlling input/output of data from/to the external system and for **temporarily storing write data into the first nonvolatile memory from the external system in the volatile memory and then transferring the write data from the volatile memory to the first nonvolatile memory**, and the consecutive address generation means and the sector address storage means for outputting the physical sector address and the consecutively generated addresses to the first nonvolatile memory and the volatile memory when data at the physical sector address is output from the first nonvolatile memory or

when data at the physical sector address is input to the volatile memory." This passage again describes use of volatile memory as a write buffer and has no apparent relationship to the subject matter of claim 20. Clarification of the rejection is respectfully requested.

The passing mention of "application" in col. 6 refers to a field of deployment for the system and does not refer to an application program.

The Office Action cites (p. 15) Li at col. 6, lines 31-37 as providing an application program interface. The application program interface 125 is described in this passage exclusively in the context of nonvolatile memories (device module 135, Fig. 3, listing mini disk, hard disc, flash ROM, CD ROM, tape). As a result, the proposed combination does not and cannot render unpatentable the subject matter recited in claim 20.

The rejections based on combinations of elements taken from Li and Tobita, and the rejection of claims 2, 20 and 21, fail to meet the standards for a finding of unpatentability set forth in MPEP §2143, entitled "Basic Requirements of a Prima Facie Case of Obviousness" (see also MPEP §706.02(j), §2141 et seq. and §2142), as was explained in the Response dated Dec. 23, 2003 with respect to all of the unpatentability rejections. Further, the Office Action identifies no teaching whatsoever in Li or Tobita of the subject matter recited in these claims. Additionally, there is no teaching or disclosure, or guidance, suggestion or motivation identified in the references or by the Office Action to attempt to combine or modify, or to aid one of ordinary skill in picking and choosing elements from the diverse embodiments of the references or in assembling those elements to attempt to arrive at the subject matter of any of Applicant's claims. As

such, the rejection appears to employ an inappropriate 'obvious to try' standard of unpatentability.

Such is improper, as is discussed below in more detail with reference to MPEP §2145(X)(B), entitled "Obvious To Try Rationale". This MPEP section states that "The admonition that 'obvious to try' is not the standard under §103 has been directed mainly at two kinds of error. In some cases, what would have been 'obvious to try' would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful. In others, what was 'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it." *In re O'Farrell*, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted)".

In this instance, no guidance in selecting some but not others of the many elements from the many embodiments of the references is identified. Similarly, no direction as to which of many possible choices is likely to be successful has been identified.

As there is no basis for the Examiner's contentions within the cited references, the only possible motivation for these contentions is hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for combining and/or modifying the teachings of the cited references. The Examiner is reminded that hindsight reconstruction is not an

appropriate basis for a §103 rejection. (See, e.g., *Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) (explaining that hindsight reconstruction is an improper basis for rejection of a claim).)

For at least these reasons, the rejection of claims 2, 20 and 21 is defective and should be withdrawn, and claims 2, 20 and 21 should be allowed.

Chen describes a "microcontroller virtual memory system and method" (Title). More specifically, Chen states (Abstract) that:

> A microcontroller memory system that provides on-chip, non-volatile memory for internal data and program code storage in such a manner that all on-chip, non-volatile memory is efficiently utilized. In one embodiment, a microcontroller memory scheme allows internal program code and data stored in the non-volatile memory to be reprogrammed in place by software executing on the microcontroller or by external devices through the microcontroller's serial port. In another embodiment, data and program code stored in the internal program area can be accessed using any instruction employed to access via an internal data bus the contents of an on-chip, volatile memory. The non-volatile memory used to store the program code and internal data can be implemented with Flash memory or EEPROM. To enable compatibility with conventional 8051 controllers, a flag in a special function register is provided that indicates whether a memory access is to be into the non-volatile memory or, in the conventional manner, into internal volatile or external volatile memory used for data (as opposed to program) storage.

In contrast, independent claim 10 recites: "An integrated circuit (IC) module comprising: a processor; volatile memory operatively coupled to the processor, the volatile memory storing volatile data in at least one data file; nonvolatile memory operatively coupled to the processor, the nonvolatile memory storing nonvolatile data in at least one data file; a memory region directory to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory; and a file location specifier to specify a physical location of

the requested data file within the volatile memory or the nonvolatile memory identified by the memory region directory as containing the requested data file", which is not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination.

Nobakht describes a "system server for channel-based internet network" (Title). More specifically, Nobakht states (Abstract) that:

> A system server for a channel-based network including one or more Internet sites and one or more user terminals. The system server includes a channel table database storing a master channel table that includes a list of channel numbers, each channel number having an associated Internet address and an associated Internet site name. Each Internet site of the network is addressable by an associated Internet address stored in the master channel table. The system server includes a network database and an update manager database. The system server identifies each user terminal requesting service by comparing transmitted identification information with authorized user information stored in the network database. The system server also compares a channel table version number from the requesting user terminal with a version number stored in the update manager database that is associated with the master channel table, and notifies each requesting user terminal when updated channel table information is available. At each user terminal, a user reads the channel numbers and associated Internet site names from a menu displaying the downloaded channel table, selects an Internet site name from the displayed menu, and enters the channel number associated with the selected Internet site name using an input device that is similar to a television remote control.

The Office Action states (p. 7) that col. 45, 66-67, col. 46, lines 1-8 and col. 47, lines 26-29 of Tobita describe "... volatile memory operatively coupled to the processor ..." and that such passages also describe "... non-volatile memory operatively coupled to the processor ...."

These passages describe a fourth embodiment with reference to Figs. 82 and 83 of Tobita. Tobita states (col. 46, line 50 et seq., that:

> Then, in the fourth embodiment, a volatile memory is adopted as the cache memory for temporarily storing data, etc., and is connected

> directly to the memory bus 4007 of the CPU 4001 and the flash memory is used as the substantial main memory. This means that **the flash memory 4002**, which is the main memory, **is not directly accessed from the CPU 4001** and therefore the slow access speed to the main memory scarcely affects the operation of the CPU 4001.

Tobita thus teaches away from coupling the nonvolatile memory to the processor. Tobita teaches that this avoids having the slow access speed to the main memory affecting the operation of the processor.

Tobita also teaches (col. 47, lines 26-29) that "Numeral 4015 is a ROM which stores a control program and numeral 4016 is a processor which executes the control program for controlling the entire information processing system of the invention. Numeral 4017 is a bus provided to transfer addresses, data, etc., within the system." This passage provides no teaching of volatile or nonvolatile memory being used to store data in one or more data files.

The Office Action also cites col. 4, lines 34-37. This portion of the teachings of Tobita is taken from the Background, which also includes col. 4, line 24 et seq., which states that:

> Whether the main memory is volatile or nonvolatile makes a great system difference.
>
> For example, when the main memory is volatile, if the system power is turned off with only the cache memory rewritten, data stored in both the main memory and the cache memory is cleared, introducing no problem. However, when the main memory is nonvolatile, if the power is turned off with the most recent data stored only in the cache memory, in fact the data just entered and still being considered by the user can disappear from the cache memory.
>
> If the main memory of an information processing system is volatile, it is common practice to provide an auxiliary storage for saving file data. However, **if the main memory system is nonvolatile**, no auxiliary storage is required. (The main memory serves as a data save area.) This point is one of the merits of the system provided with the nonvolatile main memory, but **it introduces a problem**. For example, information processing systems may career out of control due to a program error or operator mistake. When this fault

> occurs, if the main memory is volatile, it is possible to reset the hardware or, as a last resort, temporarily turn off the power and restart the system, thereby clearing the main memory contents and again loading data into the main memory from the auxiliary storage for restoring the system to the normal state. However, if the main memory is nonvolatile, when the system careers out of control and data stored in the main memory is destroyed, correct data is lost and it is difficult to restore the system to the normal state.
>
> **Therefore, the information processing systems having a nonvolatile main memory must be provided with a corrective system for crashing of the processing system.**

The point that Tobita appears to be making is that use of volatile memory results in data loss upon events such as a system crash, and that such data loss can be avoided by the use of the nonvolatile memory espoused by Tobita. Tobita describes computers that either have volatile or have nonvolatile main memory. In other words, the "OR" in the first sentence of this portion of Tobita is in the disjunctive, rather than the conjunctive, sense of that word. Tobita, again, teaches away from use of volatile **and** nonvolatile memory coupled to a processor.

The Office Action states (p. 7) that "... a memory region directory ..." is found in Tobita at col. 38, lines 19-38. Claim 10 recites "a memory region directory to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory", which is not what is cited in the Office Action.

The Office Action also states (p. 8, item 14) that "Tobita provides a processor with both volatile and nonvolatile memory, a memory region directory and file location specifier and Chen provides a flag distinguishing there data is stored in volatile or non-volatile memory." As noted above, Tobita uses volatile memory as a cache and thus recalls data only from non-volatile memory. The flag taught by Tobita cannot possibly serve as a directory.

A flag is a code denoting a specific event or the existence or status of a particular condition and is typically a single bit, i.e., has one of two possible values: ONE or ZERO. It is impossible to represent the amount of information involved in forming a memory region directory in a single bit.

Further, the definition of a directory as a flag, as is described in the Office Action, gives the term and "directory" a meaning repugnant to the ordinary meanings of these terms. Such is improper, as is described below in more detail with reference to MPEP §2111.01, entitled "Plain Meaning". This MPEP section states that:

This MPEP section states that "THE WORDS OF A CLAIM MUST BE GIVEN THEIR "PLAIN MEANING" UNLESS THEY ARE DEFINED IN THE SPECIFICATION". This MPEP section further states that "While the meaning of claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. This means that the words of the claim must be given their plain meaning unless applicant has provided a clear definition in the specification. *In re Zletz*, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)". The interpretation of the term "directory" relied on by the Examiner clearly gives this term a meaning repugnant to the ordinary meaning of the term.

The term "directory" is defined in the Microsoft Press Computer Dictionary, Third Edition (Microsoft Press, A Division Of Microsoft Corporation, Redmond, Washington, copyright 1997) at page 148 (copy enclosed) as meaning: "*n.* A catalog for filenames and other directories stored on a disk. A directory is a

way of organizing and grouping files so that the user is not overwhelmed by a long list of them. The topmost directory is called the *root directory*; the directories within a directory are called *subdirectories*. Depending on how an operating system supports directories, filenames in a directory can be viewed and ordered in various ways - for example, alphabetically, by date, by size, or as icons in a graphical user interface. What the user views as a directory is supported in the operating system by tables of data, stored on the disk, that indicate characteristics and the location of each file. In the Macintosh and Windows 95 operating systems, directories are called *folders*."

The amount of information contained in a directory, and the scope or range of such information, each exceed the limited information carrying capacity of a flag. The English term "flag" is taken from literal use of a cloth flag to have a simple, predefined meaning, while a directory, by definition, must have a greater latitude of information-carrying capacity. Accordingly, the flag employed by Chen cannot possibly substitute for a directory, as recited in claim 10. As such, the proposed combination fails to provide the subject matter of claim 10.

As noted previously, Tobita teaches away from the subject matter as recited in claim 10. Tobita teaches (col. 2, line 3 et seq.) that **directories** and FATs can cause problems because they are more frequently written to than other portions of storage media when this type of organization is employed with flash memories. Flash memories are known, to those having skill in the relevant arts, to fatigue, resulting in catastrophic failure of a memory area or cell, with repeated writes to the same memory areas. Tobita states (col. 2, line 3 et seq.) that:

> The limit of the write count mentioned above will introduce a serious problem with the use of the flash memory as storage media

> of a semiconductor disk. For example, data is written into areas such as a **directory** and FAT (file allocation table) on a disk more frequently than other areas, that is, data is frequently written into only specific blocks of the flash memory allocated to the **directory** and FAT and there is a good chance that the write count limit of the flash memory will be exceeded in the specific blocks faster than in other blocks. If the write count limit is exceeded, the elements are degraded and it may be impossible to carry out a normal read or write. If a **directory** or FAT on a disk is destroyed, the entire disk cannot be read. *Therefore, malfunction only in specific blocks makes the entire semiconductor disk unusable, leading to poor efficiency.* (emphasis added).

As such, Tobita teaches away from use of **memory directories**, as recited in claim 10. It is improper to employ a reference in a combination when the reference teaches away from the combination. This is explained more fully in MPEP 2145(X)(D)(2), entitled "References Cannot Be Combined Where Reference Teaches Away from Their Combination". This MPEP section states that: "It is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983)". In this instance, because the reference is being employed to arrive at the subject matter of the claim and because the reference teaches away from that subject matter, the reference cannot be properly employed to attempt to find unpatentability.

The Office Action states (p. 8) that "Chen teaches identifying whether data is in volatile or nonvolatile memory as follows:

"... to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory ..." at col. 6, lines 16-19." However, this is not what is recited in claim 10. Claim 10 recites "... a memory region directory to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory ...."

The cited portion of Chen states that: "The state of the NVMEN flag 242 determines whether a data memory access is into the non-volatile memory 220' or volatile memory (e.g., into of the internal data SRAM 230, SFR 240 or external data SRAM 212)." A flag is typically a single bit. Chen teaches two states, SET and CLEARED, for this flag, and states (col. 8, lines 55-58) that: "In the programming mode, the NVMEN bit is set and the MOVX (or other appropriate instructions) can be used for reconfiguring the internal program code." and that (col. 6, lines 13-15): "In one embodiment, the NVMEN flag 242 is a single bit in the SFR 240 that can be set by either external or internal programs." A single bit cannot possibly be employed to realize a memory region directory, as affirmatively recited in claim 10. Accordingly, the combination proposed in the Office Action does not provide the subject matter of claim 10.

Further, the Office Action cites diverse portions of Tobita (p. 7, item 13) as corresponding to various affirmatively-recited aspects of the subject matter of claim 10 and states (p. 8) that "Tobita does not teach identifying whether data is in volatile or non-volatile memory". The Office Action then states (p. 8, item 14) that Chen provides such teaching. The Office Action then offers the naked conclusion that "It would have been obvious ...." but fails to identify any motivation in either reference to modify and/or combine teachings.

There is no teaching or guidance identified within Tobita to aid one of ordinary skill in picking and choosing elements from the diverse embodiments of Tobita or in assembling those elements to attempt to arrive at the subject matter of any of Applicant's claims. As such, the rejection appears to employ an improper 'obvious to try' standard of unpatentability.

Such is improper, as is discussed above in more detail with reference to MPEP §2145(X)(B), entitled "Obvious To Try Rationale" (supra). In this instance, no guidance in selecting some but not others of the many elements from the many embodiments of Tobita is identified. Similarly, no direction as to which of many possible choices is likely to be successful has been identified.

As there is no basis for the Examiner's contentions within the cited references, the only possible motivation for these contentions is improper hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for combining and/or modifying the teachings of the cited references.

Additionally, independent claim 18 recites: "A file system for an integrated circuit module, comprising: means for handling a request for a data file stored on the integrated circuit module; means for identifying whether the data file is located in volatile memory or nonvolatile memory; and means for specifying a physical location of the data file within the volatile memory or the nonvolatile memory", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (p. 8) Tobita, col. 6, lines 20-22 and col. 32, lines 5-10 as providing "... means for handling the request for a data file stored on the integrated circuit module ...." Col. 6, lines 20-22 of Tobita states that: "The nonvolatile memory not electrically erasable is used as a memory to store interface information, such as the IC card internal configuration and access format." Such cannot possibly substitute for this affirmatively-recited element.

Col. 32, lines 5-10 of Tobita states that: "In operation, when it becomes necessary to store or read file data, the host sends an access request via the host bus 2002. When file data is stored, the host specifies the logical address to store the data and transfers the data; when file data is read, the host specifies the logical address on management and requests that file data stored here should be transferred." This passage is unrelated to handling any request for any data file stored on any integrated circuit module and instead refers to transfer of within a host computer system. Clarification is respectfully requested.

The Office Action cites (p. 8; see also p. 34, item 75) col. 6, lines 16-19 of Chen with respect to "means for identifying whether the data file is located in volatile memory or nonvolatile memory". The NVMEN **flag** 240 taught by Chen is used (col. 6, line 3 et seq.) to determine whether to access an internal SRAM 234 or SFR 240 or a nonvolatile memory 220. It has no particular relationship to any data file (see, e.g., Table 1) and may be set by either internal or external programs (see line 14). Clarification is respectfully requested.

Because Tobita teaches that the volatile memory is used only as a write buffer, Tobita has no need for any means for identifying whether the data file is located in volatile memory or nonvolatile memory. Data are always written from the write buffer to the flash memory and is only accessed from the flash memory.

The cited portions of the references fail to provide the subject matter recited in claim 18. As a result, the proposed combination does not provide the elements recited in claim 18.

Claim 25 recites "A file system for an integrated circuit module, comprising: an application program interface to enable an application to access

files stored in volatile memory and nonvolatile memory; and a memory region directory to identify whether a file is stored in the volatile memory or the nonvolatile memory", while claim 39 recites "A method comprising: storing volatile data in at least one volatile data file in volatile memory; storing nonvolatile data in at least one nonvolatile data file in nonvolatile memory; receiving a request to access a particular data file; determining whether the particular data file is stored in the volatile memory or the nonvolatile memory; and locating the particular data file" and claim 42 recites "A computer-readable medium storing computer-executable instructions that, when executed on a processor, cause the processor to perform acts of: storing volatile data in at least one volatile data file in volatile memory; storing nonvolatile data in at least one nonvolatile data file in nonvolatile memory; receiving a request to access a particular data file; determining whether the particular data file is stored in the volatile memory or the nonvolatile memory; and locating the particular data file", which recitations are not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination.

The Office Action fails to identify any motivation in the references to combine, the proposed combination does not provide the subject matter recited in the claim and appears to employ an improper 'obvious to try' standard for unpatentability via improper hindsight reconstruction. Accordingly, claim 25 is patentable over the proposed combination of references.

Yet further, independent claim 28 recites "A computer-readable medium storing computer-executable instructions that, when executed on a smart card, direct the smart card to: store data in a volatile data file within volatile memory of

the smart card; and facilitate access to the volatile data file by one or more applications", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (p. 20) Tobita at col. 6, lines 52-54 and col. 7, lines 30-34 as providing "... and facilitate access to the volatile data file by one or more applications ...". As noted above, the passing mention of "application" in col. 6 is a reference to a field of deployment and not to a software application executing on a processor. As noted above with reference to claim 18, the passage in col. 7 is unrelated to handling any request for stored data files and instead relates to storage of data.

The Office Action cites (p. 17) col. 5, lines 47-55 and col. 6, lines 34-38 of Li as providing "... store data in a volatile data file within volatile memory ..." with respect to claim 39 and claim 42.

The passage from col. 6 of Li states that: "Generally, only one application is resident for a particular JVM 130. The device module 135 includes a file system which can use a mini disk, a hard disk, flash ROM, a CD-ROM and/or a tape storage device." All of these devices are nonvolatile memory devices and thus cannot possibly relate to the subject matter that they are cited with respect to. Clarification of the rejection is respectfully requested.

The passage from col. 5 of is Li reproduced below:

> In general, computer system 112 of FIG. 2 includes an address/data bus 100 for communicating information, a central processor 101 coupled with the bus for processing information and instructions, a volatile memory 102 (e.g., random access memory RAM) coupled with the bus 100 for storing information and instructions for the central processor 101 and a non-volatile memory 103 (e.g., read only memory ROM) coupled with the bus 100 for storing static information and instructions for the processor 101. Computer

> system 112 also includes a data storage device 104 ("disk subsystem") such as a magnetic or optical disk and disk drive coupled with the bus 100 for storing information and instructions and a display device 105 coupled to the bus 100 for displaying information to the computer user. System 112 can also be referred to as an embedded system.

In other words, this portion of Li describes a conventional computer system such as a personal computer. In such systems, the volatile memory is used to temporarily store information relative to a specific application, and respective portions of the nonvolatile and volatile memories are set aside for data storage.

The portions of the volatile memory that are set aside for use by a particular application are exclusively dedicated to that application. At various times, the application may write data files to the nonvolatile memory. As a result, the application generates requests to access the information that is stored in the various portions of memory, but it does not receive requests for data that would ordinarily be stored in either volatile or nonvolatile memory.

One reason that volatile memory regions are exclusively apportioned, i.e., are not used for storage of data files that may be accessed by a request such as recited in claim 39, is that when one application overwrites data in volatile memory regions that have been dedicated for exclusive use by another application, the data that had been stored by the another application are lost. Often, when this happens, the new data are so grossly incommensurate with the data formats employed by the another application that, when those regions that had been used to store such data are accessed by the another application, the another application "crashes".

When an application accidentally overwrites ("bombs") data stored in volatile memory areas employed by at least some operating system portions, and

those volatile memory areas are subsequently accessed by the operating system, the operating system "crashes". This often results in serious computer malfunction usually requiring a "re-boot" in which the computer re-initializes and then reallocates all volatile memory etc.

Against this backdrop, it is apparent that volatile memory in conventional computers is employed in such a manner that the term "volatile data file" is inapposite to such systems. Put another way, to "facilitate access to the volatile data file by one or more applications" does not comport with normal or appropriate operation of computer systems such as that described by Li. Further, the Office Action improperly ignores these arguments and yet repeats the rejection. Accordingly, the rejection of claims 39 and 42 fails to provide the elements of the claims, appears to improperly employ hindsight reconstruction via an 'obvious to try' standard and does not meet the standards for a finding of unpatentability as set forth in the MPEP.

With respect to claim 28, Nobakht is cited (p. 19) as providing "... of the smart card ...". However, this excerpt as provided in the Office Action fails to reflect the recitation of claim 28. Claim 28 recites "... computer-executable instructions that, when executed on a smart card, direct the smart card to: store data in a volatile data file within volatile memory of the smart card ...." Nobakht describes a conventional smart card 232 having a nonvolatile memory 330 (see fig. 3B; col. 6, lines 42-49) and provides no mention of any volatile memory or volatile data files in the context of the smart card 232. Nobakht fails to provide (i) execution of computer-executable instructions (ii) that, when executed on a smart

card (iii) store data in a volatile data file (iv) within a volatile memory (v) on a smart card, as recited in claim 28.

As a result, the cited references fail to provide the elements of claim 28 and the proposed combination does not reflect and cannot render unpatentable the subject matter of claim 28. Accordingly, claim 28 distinguishes over the references cited and should be allowed.

As well, independent claim 29 recites "A method for operating an integrated circuit (IC) module, comprising: receiving a request for a data file stored on the IC module; identifying, within the IC module, whether the data file is located in volatile memory or nonvolatile memory; and specifying a physical location of the data file within the volatile memory or the nonvolatile memory", while independent claim 32 recites "A computer-readable medium storing computer-executable instructions that, when executed on a processor, cause the processor to perform acts of: receiving a request for a data file stored on the IC module; identifying, within the IC module, whether the data file is located in volatile memory or nonvolatile memory; and specifying a physical location of the data file within the volatile memory or the nonvolatile memory", which recitations are not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action states (p. 7) that claims 29 and 32 stand rejected and cites portions of Tobita and Chen which have been discussed hereinabove with reference to claim 18. The Office Action also states, in surrebuttal (page 40, item 86) that "... receiving a request for a data file stored on the IC module ..." is taught by Tobita at col. 6, lines 20-22 and col. 32, lines 5-10. Col. 6, lines 20-22 states

that: "The nonvolatile memory not electrically erasable is used as a memory to store interface information, such as the IC card internal configuration and access format." This bears no apparent relationship to requests for data files or to such requests for data from any integrated circuit module. Further, this portion of Tobita deals exclusively with nonvolatile memory and thus is incommensurate with a mix of volatile and nonvolatile memory as recited in these claims.

The entirety of Tobita is void of the term "module". The passage at col. 6, lines 20-22 is reproduced hereinabove and provides no teaching at all of any data being stored within any integrated circuit module. Storage of basic input-output system data or BIOS on a ROM, which appears to be what is described in Tobita, is completely unrelated to determination of whether data are stored in volatile or nonvolatile memory in an integrated circuit module. Clarification and provision of a basis for the rejection of claim 29 is respectfully requested. As a result, the rejection of claim 29 is prima facie defective and should be withdrawn, and claim 29 should be allowed.

Independent claim 33 recites "A method comprising: storing data in a volatile data file in volatile memory of an integrated circuit module; receiving, from a requestor, a request to access the volatile data file on the integrated circuit module; evaluating whether the requestor is authorized to access the volatile data file; and in an event that the requestor is authorized, locating the volatile data file in the volatile memory", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (p. 20) Tobita at col. 6, lines 20-22 and col. 45, line 66 though col. 46, line 8 with respect to claim 33. These portions of Tobita have

been discussed above with reference to the rejection of claim 18 and claim 20. The Office Action also cites col. 7, lines 3-5. This passage is exclusively devoted to storage of data in flash (nonvolatile) memory. However, claim 33 recites "... storing data in a volatile data file in volatile memory ...." and thus is unrelated to that aspect of Tobita.

The Office Action also cites (p. 20) col. 31, lines 32-35 of Tobita with reference to access of a volatile data file. As noted above with respect to claim 20, col. 31, lines 32-54 of Tobita describes temporary use of SRAM as a write buffer 2006 to aid in the speed with which files can be transferred from a host to flash memory and does not describe a volatile data file or such that can be accessed. The Office Action further cites col. 45, line 66 through col. 46, line 8, which has been previously discussed supra. These passages are non sequitur with respect to any volatile data file or access thereto.

The Office Action further cites (p. 20) col. 46, lines 59-66 of Tobita as providing "... locating the volatile data file in the volatile memory ...". Col. 46, line 59 et seq. states that:

> Referring again to FIG. 82, the CPU 4001 accesses the cache memory 4003 via the memory bus 4007. The access address is input to the address comparison circuit 4005, which then compares the address with addresses previously registered in the address array 4004. If the address matches one of the registered addresses, which will be hereinafter referred to as an "address hit," the controller 4006 accesses the location in the cache memory 4003 corresponding to the address. In contrast, if the address does not match any of the registered addresses, which will be hereinafter referred to as an "address miss," the controller 4006 registers the address in the address array 4004. After this, the controller 4006 transfers the data corresponding to the address to the cache memory for storage and accesses the location in the flash memory 4002 corresponding to the address.

Consonant with the above description, cache memories are not generally used to store data files and the above passage certainly does not describe or suggest such. Cache memories typically are limited-capacity but very high speed memories that are very tightly coupled to a processor. Cache memories are used to store addresses and/or data elements and/or instructions that are repeatedly demanded by the processor. Cache memories are employed for these purposes and within this operational purview because this can significantly reduce memory access time, particularly with tasks involving repetitive processor instructions or memory accessions, and thus increase overall system operation speed. Storing data files in a cache memory completely defeats their intended purpose. Employing a reference in a manner that defeats its intended purpose is improper, as is explained below in more detail with reference to MPEP §2143.01, entitled "Suggestion or Motivation to Modify the References".

In a subsection entitled "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE", this MPEP section states that: "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) ...."

Inasmuch as modifying these teachings to arrive at the subject matter of the claim or attempting to adapt the teachings of Tobita for such renders the teachings the reference unsatisfactory for their intended purpose, there is, as a matter of law, no motivation to modify the teachings of Tobita as suggested by the Office Action.

Accordingly, the rejection of claim 33 should be withdrawn, and claim 33 should be allowed.

Independent claim 39 recites "A method comprising: storing volatile data in at least one volatile data file in volatile memory; storing nonvolatile data in at least one nonvolatile data file in nonvolatile memory; receiving a request to access a particular data file; determining whether the particular data file is stored in the volatile memory or the nonvolatile memory; and locating the particular data file", which is not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The cited portions of Tobita and Chen have been discussed above. The Office Action cites (p. 17) Li (col. 5, lines 47-55) for "storing volatile data in at least one volatile data file in volatile memory; storing nonvolatile data in at least one nonvolatile data file in nonvolatile memory", as recited in claim 39. This passage is discussed above with reference to claim 28 and fails to provide the subject matter recited in claim 39.

To put the discussion of this passage into the context of claim 39, the system described in Li would not require "determining whether the particular data file is stored in the volatile memory or the nonvolatile memory" in response to "receiving a request to access a particular data file". When such a system receives a request to access a particular data file, that data file is fetched from nonvolatile memory, such as a disc or optical drive.

Accordingly, the rejection of claim 39 is prima facie defective and should be withdrawn, and claim 39 should be allowed.

As well, independent claim 38 recites "A computer-readable medium storing computer-executable instructions that, when executed on a processor, cause the processor to perform acts of: storing data in a volatile data file in volatile memory of an integrated circuit module; receiving, from a requestor, a request to access the volatile data file on the integrated circuit module; evaluating whether the requestor is authorized to access the volatile data file; and in an event that the requestor is authorized, locating the volatile data file in the volatile memory", while independent claim 43 recites "A method comprising: storing data produced by a first application within a volatile data file within volatile memory in a smart card; and accessing the volatile data file from a second application" and claim 45 recites "A computer-readable medium storing computer-executable instructions that, when executed on a processor, cause the processor to perform acts of: storing data produced by a first application within a volatile data file within volatile memory in a smart card; and accessing the volatile data file from a second application" which recitations are not taught, disclosed, suggested or motivated by the cited references, alone or in combination.

The Office Action cites (pp. 20, 21) portions of Tobita whose deficiencies are addressed above with reference to claim 18 and portions of Li whose deficiencies are addressed above with reference to claim 39. Nobakht's references to smart cards fail to cure these deficiencies. Accordingly, the rejection of claims 38, 43 and 45 is in error and should be withdrawn, and claims 38, 43 and 45 should be allowed.

Claim 46 recites "An integrated circuit (IC) module comprising: a processor; a memory system operatively coupled to the processor, the memory

system including: volatile memory; electrically reprogrammable nonvolatile memory; read-only memory configured to provide an operating system and a file management system, wherein the file management system is configured to manage access to one or more data files stored in the volatile memory, the nonvolatile memory or the read only memory, wherein the file system includes an access control table configured to restrict access to portions of the memory system to authorized applications", which is not taught, disclosed, suggested or motivated by the cited references, alone or in any proper combination.

The Office Action cites (p. 22, item 54) portions of Tobita discussed hereinabove and proposes to combine these with elements taken from widely-varying portions of Ginter. The combination fails to provide the subject matter of claim 46, and the Office Action identifies no suggestion or motivation in the references to motivate such selection or to aid one in determining which bits and pieces to select or to show how to combine them. As such, the Office Action again appears to be employing an 'obvious to try' standard for finding unpatentability coupled with improper hindsight reconstruction.

Further, simply providing a conclusory statement that "It would have been obvious ...." fails to meet the standards set forth in the MPEP for establishing a prima facie case of unpatentability. These are set forth in MPEP §2143, entitled "Basic Requirements of a Prima Facie Case of Obviousness" (see also MPEP §706.02(j), §2141 et seq. and §2142).

This MPEP section states that "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge

generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." The references fail to teach or disclose the elements recited in the claims, as noted with specificity hereinabove. Accordingly, the references cannot possibly provide motivation to modify their teachings to arrive at the invention as claimed, and the Examiner has identified no such teaching or disclosure in the references. As a result, the first prong of the test cannot be met.

MPEP §2143 further states that "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Inasmuch as the references fail to provide all of the features recited in Applicant's claims, as noted with specificity hereinabove, the third prong of the test is not met. As a result, there cannot be a reasonable expectation of success. As such, the second prong of the test cannot be met.

MPEP §2143 additionally states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." This fourth criterion cannot be met because the references fail to teach or disclose the elements recited in the claim. As such, the unpatentability rejections fail all of the criteria for establishing a prima facie case of obviousness as set forth in the MPEP.

Moreover, no evidence has been provided as to why it would be obvious to combine or modify the teachings of these references. Evidence of a suggestion to combine or modify may flow from the prior art references themselves, from the

knowledge of one skilled in the art, or from the nature of the problem to be solved. However, this range of sources does not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

Dependent claims 2-9, 11-17, 19, 21-24, 26, 27, 30-31, 34-37, 40, 41, 44 and 47-53 distinguish for their own recited features and/or by virtue of dependence from allowable claims. Accordingly, the unpatentability rejection of claims 2-6 and 8-53 is defective and should be withdrawn, and claims 2-6 and 8-53 should be allowed.

Response to Surrebuttal

The Office Action states (p. 36) that "The Examiner has chosen to interpret Tobita's use of the word application to mean one or more programs for implementation of access to these various types of memories." However, this clearly is not an appropriate interpretation of the term as it is used by Tobita. More specifically, the cited passages, taken in context, state (col. 4, line 58 et seq.) that: "It is therefore an object of the invention to provide a file system using a high-performance and inexpensive flash memory as storage media", a plain statement of intent to employ nonvolatile memory as storage media. Col. 6, line 49 et seq. states that:

> If the nonvolatile memory not electrically erasable is used to store IC card information, it is made possible to be compliant with the PCMCIA specifications (standard specifications), etc. If all the above-mentioned points are implemented, the three types of memory can cover various **applications** and the number of parts can be reduced compared with installation of a memory for each **application**. Particularly in intending miniaturization for IC cards, etc., it contributes greatly to reduction of the number of parts.
>
> According to the invention, there is further provided a flash memory system comprising a flash memory for storing data from an external system, means for temporarily storing the data from the external system upon receipt of a request to write the data into the flash memory, and a control section which stores the data in the data storage means upon receipt of the request to write the data, then transfers the data to the flash memory, wherein upon receipt of a request to read or write data from the external system before completion of transfer of the data to the flash memory, the control section interrupts the data transfer to the flash memory and responds to the request to read or write the external data.

The sense in which the word "application" is being used by Tobita clearly corresponds to "field of use". Those of skill in the relevant arts will understand that one does not ordinarily contemplate "installation of a memory for each application" when the word "application" is used to refer to software products.

Transformation of a statement of intended fields of use, to an "application program" and then to an "application program interface" simply misinterprets the teachings of the reference. Such is improper, misdescriptive and misleading to the public.

The Office Action states (p. 37, item 80) that "Li teaches the use of both volatile and non-volatile memories. The application program interface described by Li could be used with both types of memory." Li, however, states (col. 6, lines 31-37) that: "Within the system architecture 120 of FIG. 3, the API layer 125 or application program interface is shown as the top layer. The API 125 is associated with a JVM 130. Generally, only one application is resident for a particular JVM 130. The device module 135 includes a file system which can use a mini disk, a hard disk, flash ROM, a CD-ROM and/or a tape storage device."

The Office Action also states (p. 29, item 67) that Tobita teaches "a memory region directory" and that Chen teaches "to identify whether a requested data file is located in the volatile memory or in the nonvolatile memory", and then contradicts this conflation by stating that "Chen actually teaches the use of a flag for this purpose. However, thus function may also be stored in the memory region directory taught by Tobita."

The Office Action also states (p. 30, item 68) that "Tobita teaches use of a memory management table, which serves as a directory for memory block use as follows" and then repeats a portion of Tobita found at col. 38, lines 19-38.

This passage also refers to use of single bits as flags to denote whether a given block of memory has been used. As noted above, it is impossible for a single bit flag to represent the amount of information contained in a directory

entry for even a single file. Put another way, computer memory address busses are typically several bytes wide and thus a memory address or a description of file location cannot be represented by a single bit or flag.

The Office Action states (p. 31, item 69) that "The applicants have suddenly jumped from their discussion of independent claim 10 to claim 13, which is dependent on claim 10. The use of FATS tables is well known in the state of the art." Such interpretation is erroneous.

To assist with the confusion evidenced by this statement in the Office Action, Applicant notes that a portion of such confusion appears to result from conflation of the legal argument being presented with the technical content of the reference. The legal discussion relative to claim 10 focuses on a legal concept known as "teaching away", which the Office Action fails to address.

"Teaching away" is a legal doctrine whereby a reference fails to function to provide or support unpatentability because the reference teaches that the subject matter of the claim is undesirable in the context of the problems being addressed by the reference. Because Tobita teaches away from the subject matter of claim 10, it is improper, as a matter of law, to attempt to modify the teachings of Tobita in an effort to find unpatentability.

The Office Action states (p. 33, item 73) that "Tobita teaches means for handling a request for a data file stored on the integrated circuit module" at col. 32, lines 5-10 and col. 6, lines 20-22 ...." These passages are void of any reference whatsoever to data of any sort stored on any integrated circuit module. The Office Action further states (p. 33, item 73) that "Chen teaches "means for identifying whether the data file is located in volatile memory or nonvolatile

memory" at col. 6, lines 16-19 ...." This passage, as noted above, has no particular relationship to any data file. The Office Action continues on to state that "Tobita teaches "means for specifying a physical location of the data file within the volatile memory or the nonvolatile memory" at col. 5, lines 27-63."

This passage describes a computer system having various computer components, and is followed (line 64 et seq.) by a passage that states that:

> In the invention, the data store unit is made the same as one sector of hard disk. Data is always transferred in sector units to and from the host. To transfer the data at high speed, means for generating addresses at high speed is provided. To match the write speed with the high-speed address generation, the nonvolatile [sic] memory is used as a write buffer, and all write data is temporarily stored in the write buffer. The write buffer is used to temporarily save data. After data transfer from the host terminates, the data is transferred from the write buffer to the flash memory quickly. That is, the write buffer is not used to prolong the flash memory life and is used **only** for high-speed data transfer. The flash memory life is prolonged, for example, by managing the erasure count. The erasure count is recorded as the second management information in flash memory erasure units. How much the flash memory is degraded is decided according to the erasure count and write locations are determined for averaging progress of degradation. Thus, the erasure counts are recorded in the volatile memory used for the write buffer.

In the rebuttal on page 34, item 74, the Office Action again cites col. 32, lines 5-10 of Tobita. As noted above, neither this passage nor Chen teach, alone or in any proper combination, teach, disclose, suggest or motivate the subject matter of claim 18.

The portion (col. 38, lines 19-38) of Tobita cited (p. 17) as providing "... and a memory region directory ..." is directed to tables 3205 and 3206 for storing address information relative to a flash (**nonvolatile**) memory 3106 divided into portions such as 3108 and 3109 (see col. 37, line 38 et seq.) and are unrelated to "a memory region directory to identify whether a file is stored in the volatile memory

or the nonvolatile memory", as recited in claim 25. The passage referenced (p. 16, item 36, Office Action) in Li (col. 6, lines 31-38) is discussed above with reference to claim 20.

The Office Action reiterates (p. 37, item 81) that the recitation of claim 25 is taught by combining the teachings of Tobita, Li and Chen. The Office Action fails to identify any motivation in the references to combine, the proposed combination does not provide the subject matter recited in the claim and appears to employ an improper 'obvious to try' standard for unpatentability via improper hindsight reconstruction.

The Office Action states (p. 38) that "The Examiner has chosen to interpret Tobita's use of the word application to mean one or more programs for the implementation of access to these various types of memories." Tobita uses the word "application exactly thirteen times. The first use of the word "application" relates to foreign priority. The second through seventh instantiations refer to provenance data.

The eighth and ninth (col. 6, lines 53 and 54) clearly deal with a range of applications for the information processing system and are the instance that is mischaracterized in the Office Actions. The tenth (col. 49, line 52) makes reference to a flash memory application, i.e., consistent with how Applicant has characterized the usage of the term. The eleventh appearance of this term (col. 34, lines 14-16) appears to describe application of the disclosure associated with Fig. 53 to another use. The twelfth (col. 48, lines 42 and 43) clearly refers to application of a well-known set associative method. The thirteenth (col. 49, lines 51 and 52) refers to application of a memory to a task.

Not one of these instantiations employs the word "application" in the manner in which the Examiner is choosing to interpret the usage of the word, yet Tobita contains 60 columns of specification directed to application of flash memories. Tobita consistently refers to execution of tasks by a CPU and frequently employs the term "flow" with reference to a sequence of computer-executed tasks (see, e.g., col. 15, lines 45 and 46, stating that "FIG. 42 is a sequence flow of garbage collection according to first embodiment of the present invention"; Tobita makes numerous other references to flow etc.).

Tobita is a lengthy document taking priority from a number of Japanese applications and lists a number of inventors who are resident in Japan. As a result, one might realize that the party or parties who prepared the English language specification were not native English speakers and may well not even be familiar with the interpretation of the term "application" as it is being interpreted in the Office Action. Put another way, there is no credible evidence in support of the strained interpretation offered in the Office Action and there is substantial credible evidence for Applicant's interpretation of the usage of the term.

The Office Action also states (page 41, item 87) that Tobita teaches "within the IC module" at col. 6, lines 20-22. The entirety of Tobita is void of the term "module". The passage at col. 6, lines 20-22 is reproduced hereinabove and provides no teaching at all of any data being stored within any integrated circuit module. Storage of basic input-output system data or BIOS on a ROM, which appears to be what is described in Tobita, is completely unrelated to determination of whether data are stored in volatile or nonvolatile memory in an integrated circuit module.

The Office Action states (pages 41 and 42) that "The common theme of all three inventions is that they are providing access to memory, which fits with the proposed invention, which is providing access to both volatile and nonvolatile memory". However, this completely ignores the argument made by Applicant, that adapting the teachings of Tobita as suggested renders those teachings unsuitable for their intended purpose. The Office should respond to the legal argument being set forth by Applicant in the event that the Office persists with the same inapposite rejection.

Examination Deficiencies

Additionally, the Examiner's response to argument is deficient in multiple regards. A first deficiency is that the anticipation rejection is defective and the Examiner has not responded adequately to the anticipation traverse provided by Applicant. The response to argument clearly fails to respond to Applicant's arguments with respect to the rejections under 35 U.S.C. §102, or, in the alternative, is an admission that these rejections are defective.

Applicants note the requirements of MPEP §707.07, entitled "Completeness and Clarity of Examiner's Action". This MPEP section cites 37 CFR §1.104, entitled "Nature of examination" which in turn states, in subsection (b), entitled "Completeness of examiner's action" that "The examiner's action will be complete as to all matters, except that in appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters before further action is made."

This MPEP section further states, under a heading labeled "Examiner Note" that "The Examiner must, however, address any arguments presented by the applicant which are still relevant to any references being applied." The Office Action clearly fails to comport with these requirements as set forth in the MPEP, at least because the Office Action both fails to address Applicant's arguments with respect to anticipation and continues to reject claims as being anticipated.

A second deficiency is that the §103 rejections continue to fail to comport with appropriate examination guidelines. The Examiner has ignored these guidelines without providing any appropriate legal basis for doing so, and has

misinterpreted and mischaracterized the teachings of the references in making the rejections.

A third deficiency is the failure to respond to all arguments traversing the anticipation and unpatentability rejections. The response to argument clearly fails to respond to Applicant's arguments with respect to the rejections under 35 U.S.C. §102 or 103, or, in the alternative, is an admission that these rejections are defective.

Merely stating conclusions regarding the features recited in the claims without appropriate legal reasoning does not constitute a basis for rejection of the claims, particularly when the reference fails to provide the features recited in the claims and the rejections fail to meet the standards for such rejections as set forth in the MPEP and as demonstrated by Applicant.

For at least these reasons, the Office Action fails to comport with appropriate standards for examination. The Examiner should either allow Applicant's claims or provide a meaningful basis for rejection and an appropriate response to Applicant's arguments.

Conclusion

Claims 1-6 and 8-53 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

Date: July 30, 2004

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